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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,622	10/26/2005	Yuichi Takamine	36856.1376	7411
54066 7590 12/18/2007 MURATA MANUFACTURING COMPANY, LTD. C/O KEATING & BENNETT, LLP 8180 GREENSBORO DRIVE SUITE 850 MCLEAN, VA 22102			EXAMINER SUMMONS, BARBARA	
			ART UNIT 2817	PAPER NUMBER
			NOTIFICATION DATE 12/18/2007	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	Application No. 10/554,622	Applicant(s) TAKAMINE, YUICHI	
	Examiner Barbara Summons	Art Unit 2817	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 September 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6-25 is/are pending in the application.
- 4a) Of the above claim(s) 14-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-8 and 10-12 is/are rejected.
- 7) ☒ Claim(s) 9 and 13 is/are objected to.
- 8) ☒ Claim(s) 6-25 are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 October 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/26/05</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of the invention of Group I, claims 6-13, in the reply filed on 9/26/07 is acknowledged.
2. Claims 14-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention (Group II), there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/26/07.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6, 8 and 10-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. JP 2003-032061 (cited by Applicant) taken together with Suzuki JP 55-041048 (cited by Applicant), wherein either reference can be modified by the other such that there is not a "primary" reference per se.

Regarding claims 6, 10 and 12, Kobayashi et al. discloses a surface acoustic wave (SAW) filter (see section [0002]) comprising: a mount board 5 (see Figs. 1 and 3) including a land 6a; a device chip 4 (Fig. 3) in which a wiring pattern including an interdigital transducer/IDT 2b and a pad 2a electrically connected to the IDT 2b is

provided on one principal surface of piezoelectric substrate 8 (see Fig. 1 and section [0009]) of lithium tantalate or lithium niobate (see section [0012]), the pad 2a being disposed so as to oppose the land 6a of the mount board 5, the pad 2a and the land 6a being electrically connected through a bump 3 that is gold (see section [0014]); and a resin film 7 (see Fig. 4) covering the other principal surface of the piezoelectric substrate 8 sealing the device chip 4.

However, Kobayashi et al. does not disclose that the one principal surface of the piezoelectric substrate with the IDT and pad has an area greater than the area of the other principal surface of the piezoelectric substrate, by a tapered portion extending along an outer edge of the other principal surface of the piezoelectric substrate, or the land being made of gold.

Regarding claims 6, 8 and 10, Suzuki discloses (see Fig. 5) a SAW transversal filter with IDTs 12 and 13 on a piezoelectric substrate 11 of lithium tantalate or lithium niobate (see e.g. page 261, col. 2, line 1), wherein the piezoelectric substrate has a one principal surface on which the IDTs are formed that has a larger area than the other principal surface of the piezoelectric substrate, by means of a tapered portion extending along an outer edge of the other principal surface of the piezoelectric substrate 11 in order to provide the benefit of suppressing spurious responses due to reflections at the edges of the piezoelectric substrates.

However, Suzuki does not disclose a specific package for its SAW device chip.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the SAW filter of Kobayashi et al. (see Figs. 1, 3

and 4) by having replaced the rectangular piezoelectric substrate 8 device chip 4 of Kobayashi et al. with a piezoelectric substrate having a one principal surface on which the IDTs are formed having a larger area than the other principal surface by means of tapered edges of the piezoelectric substrate as suggested, for example, by the exemplary teaching thereof by Suzuki (Fig. 5), because such an obvious modification would have provided the advantageous benefit of reduced spurious responses due to the undesirable reflections of the acoustic waves at the edges of the piezoelectric substrate, as explicitly suggested by Suzuki (see the abstract, lines 1-4 and the last 7 lines thereof). Regarding the use of a gold land on the mounting board, Kobayashi et al. is silent as to the material of the land, thereby suggesting to one of ordinary skill in the art that any well known circuit conductor, such as gold, would have been usable therewith, and because gold would have been a well known art recognized alternative to any other conductor used, and wherein gold to gold bonding with the gold bump 3 of Kobayashi et al. would have been extremely well known by those of ordinary skill in the art of face down mounting of SAW devices.

It would have been equally obvious to one of ordinary skill in the art at the time the invention was made to have modified the SAW device of Suzuki (Fig. 5) by having mounted it face down on a mounting board by bump bonding and sealed it with a resin as suggested by the exemplary teaching thereof by Kobayashi et al., because SAW devices necessarily require sealing to protect them from environmental factors, and because Suzuki is silent as to the specific type of packaging used, thereby suggesting to one of ordinary skill in the art that any well known package be used, such as the face

down mounted and resin sealed package of Kobayashi et al. which would have provided the advantageous benefits of reduced size and cost vs. conventional packages with lids as explicitly suggested by Kobayashi et al. (see sections [0003]-[0007]), and as would have been known by one of ordinary skill in the art. Note that the use of gold bumps and mounting board lands would have been obvious art recognized alternative circuit conductor materials as discussed above.

5. Claims 6, 7 and 10-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. JP 2003-032061 (cited by Applicant) taken together with Takezaki et al. JP 60-176317 (cited by Applicant).

Kobayashi et al. discloses the invention as discussed in the immediately preceding rejection.

However, regarding claims 6 and 7, Kobayashi et al. does not disclose the piezoelectric substrate having one principal surface on which the IDTs are formed having a larger area than the other principal surface due to a step at the side edge of the piezoelectric substrate.

Takezaki et al. discloses such a piezoelectric substrate device chip 5 in Fig. 2(d), which also provides the benefit of reduced spurious responses due to acoustic wave reflection at the edges of the piezoelectric substrate (see the abstract, lines 1-3), but does not disclose a specific package for the SAW transversal filter device (see Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the SAW filter device of Kobayashi by

having used a piezoelectric substrate with a step at the edges, as suggested by the exemplary teaching thereof by Takezaki et al. [see Fig. 2(d)], in place of the rectangular piezoelectric substrate chips of Kobayashi et al. because such an obvious modification would have provided the benefit of reduced spurious responses due to acoustic wave reflections at the edges of the substrates as explicitly suggested by Takezaki et al. (see the abstract, lines 1-3). Note that the use of gold mounting board lands would have been obvious for the same reasons given in the immediately preceding rejection.

It would have been equally obvious to one of ordinary skill in the art at the time the invention was made to have modified the SAW filter device of Takezaki et al. with a piezoelectric substrate with a step at the side edge, by having packaged it via face down mounting on a board and sealing with resin, because SAW filter devices necessarily require packaging, wherein Takezaki et al.'s silence as to the type of packaging would have suggested to one of ordinary skill in the art that any well known package would have been usable therewith, and because the face down mounted resin sealed package would have provided the benefits of reduced size and cost over conventional packages with lids, as explicitly suggested by Kobayashi et al. (see sections [0003]-[0007]).

***Allowable Subject Matter***

6. Claims 9 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, while the prior art of record does disclose rounded/curved edges of piezoelectric substrates, in these substrates the two principal surfaces of the piezoelectric substrate appear to have the same area, not the principal surface on which the IDTs are formed having an area "greater than an area of the other principal surface of the piezoelectric substrate" as also required by claim 1 (see the last two lines thereof). Regarding claim 13, the recited thickness of the step is not disclosed or suggested by the prior art of record.

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sone JP 62-257210 discloses a SAW resonator filter (Fig. 2) having a curved edge (see Figs. 1 and 5 and the abstract, lines 1-4), but it is curved such that the principal surface of the piezoelectric substrate on which the IDT is formed has a smaller, not greater, area than the other principal surface (see Fig. 1).

Judd et al. U.S. 3,781,721 discloses a SAW transversal filter with a piezoelectric substrate having curved edges, but its principal surfaces appear to be the same size.

Nakatani et al. U.S. 2002/0159242 is cited to provide evidence that SAW packaging and semiconductor chip packaging are interchangeable (see e.g. the abstract, lines 1-3).



Yamada et al. U.S. 6,570,469 is cited to show that both SAW filter device chips and semiconductor device chips are known to be packaged by face down mounting and resin sealing (see Fig. 2 and col. 8, lines 38-40) even on the same mounting board.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barbara Summons whose telephone number is (571) 272-1771. The examiner can normally be reached on M-Th, M-Fr.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bob Pascal can be reached on (571) 271-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bs  
December 11, 2007

  
**BARBARA SUMMONS**  
**PRIMARY EXAMINER**